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Description

Bandwidth Limited Sampling Circuit of High Linearity

Cross Reference to Related Applications

[0001] The present application is related to and claims priority from co_pending US provisional patent application entitled, "Noise Suppression Scheme for Sampling Circuit", Filed on: 08/29/2003, Serial Number: 60/498,801, Attorney Docket Number: TI-919PS, naming as inventors: AYYAGARI et al, and is incorporated in its entirety herewith into the present application.

Background of Invention

[0002] *Field of the Invention*

[0003] The present invention relates to the design of electrical/electronic circuits, and more specifically to a method and apparatus for attaining a bandwidth limited sampling circuit of high linearity.

[0004] *Related Art*

[0005] A sampling circuit generally refers to a component which samples a signal level of an input signal (e.g., analog signal) at a particular instant of time and provides an output signal having the signal level to other components for a long duration. In general, a sampling circuit samples an input analog signal at a time point specified by a clock signal, and provides an output signal with the sampled strength to other components for further processing for a long time.

[0006] An input signal generally contains a source signal and a noise signal/component. It is generally desirable that the sampled output generated by a sampling circuit contain only the source signal component, which is generally referred to as providing a high signal to noise ratio (SNR).

[0007] A prior approach may remove the noise component by eliminating high frequency components from an input signal as the noise component is generally present at high frequencies. One problem with such an approach is that some of the components performing such removal may have non_linear characteristics, which results in a non_linear response in terms of the overall sampling operation. The non_linearity is undesirable in several environments. Accordingly, what is needed is a bandwidth

limited sampling circuit of high linearity providing high SNR.

Brief Description of Drawings

[0008] The present invention will be described with reference to the following accompanying drawings.

[0009] Figure (Fig.)1 is a block diagram illustrating an example environment in which the present invention may be implemented.

[0010] Figure 2 is a block diagram of an analog front end illustrating the details (in one embodiment) as relevant to an understanding of several aspects of the present invention.

[0011] Figure 3 is a circuit diagram illustrating the details of a sampling circuit in one prior embodiment.

[0012] Figure 4 is a circuit diagram illustrating the details of a sampling circuit in an embodiment of the present invention.

[0013] Figure 5 is a circuit diagram illustrating the details of a sampling circuit in an alternative embodiment of the present invention.

[0014] Figure 6 is a circuit diagram illustrating the details of a correlated double sampler (CDS) used as a sampling circuit in a CCD sensor in one embodiment.

[0015] In the drawings, like reference numbers generally indicate

identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

DETAILED DESCRIPTION

[0016] *1. Overview*

[0017] A sampling circuit implemented according to one aspect of the present invention contains a first circuit portion which limits the bandwidth of an input signal containing both source signal and a noise signal, and a second circuit portion samples the bandwidth limited signal. Noise signal, which is generally of high frequency, is substantially absent at an output of the sampling circuit due to the operation of the first circuit portion. As a result, the immunity of the output signal generated by the sampling circuit to noise is enhanced. In one embodiment described below, the first circuit portion is implemented as a R_C circuit operating as a low pass filter, and the second circuit portion is implemented using a switched capacitor.

[0018] According to another aspect of the present invention, the sampling circuit is implemented using two paths, with the first circuit path sampling the input signal (including

source signal and noise signal) and the second circuit path sampling only the high frequency components of the input signal. The sampled signal is generated as a difference of the signals sampled by the two paths. Due to the difference, any high frequency noise components are eliminated, thereby enhancing the immunity of the output signal of the sampling circuit to the noise in the input signal.

[0019] Various aspects of the present invention are described below with reference to an example problem. Several aspects of the invention are described below with reference to examples for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide a full understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details, or with other methods, etc. In other instances, well_known structures or operations are not shown in detail to avoid obscuring the invention.

[0020] *2. Example Environment*

[0021] Figure 1 is a block diagram illustrating an example environment in which the present invention can be implemented. Light 119 emanating from image 110 is shown

being passed to device 190 (such as a digital camera or a scanner). Device 190 generates pixel data elements representing image 110. The pixel data elements may be forwarded on path 168, and used in several ways, for example, viewed/edited by computer system 180_1, stored in floppy disk 180_2, printed on printer 180_3 or transferred to video player 180_4.

[0022] Device 190 is shown containing lens 120, CCD (Charge Coupled Device) 130, analog front end (AFE) 140 and post processor 160. Light 119 from image 110 is shown being focused on CCD 130 by lens 120. CCD 130 contains several pixels which are charged proportionate to the product of the intensity of the incident light and the time of exposure to the light. The charge (example of an electrical signal) is converted into voltage in a known way and transferred to AFE 140 on path 134.

[0023] AFE 140 converts an input signal received on path 134 into digital values (on path 146) representing the image, and transmits the digital values to post processor 150. Input signal on path 134 may contain a source signal representing the voltages and an unwanted noise signal. AFE 140 may employ techniques such as correlated double sampling (which are well known in the relevant arts) in the

course of generating the digital values while substantially eliminating the noise signal in the digital values in accordance with several aspects of the present invention as described below in further detail.

[0024] Post processor 160 (example of a processor) processes the digital values received on path 146, generally to enhance the quality of image represented by the digital values and/or to convert the data into suitable format for storing. The resulting output data on path 168 may be used in several ways by one of the external devices, for example, stored in a memory for processing later. The description is continued with reference to the details of example embodiment of AFE 140.

[0025] *3. Analog Front End*

[0026] Figure 2 is a block diagram of AFE 140 illustrating the details (in one embodiment) as relevant to an understanding of several aspects of the present invention. AFE 140 is shown containing sampling circuit 210, programmable gain amplifier (PGA) 220 and analog to digital converter (ADC) 230. Each component is described below in further detail.

[0027] Sampling circuit 210 samples the voltage levels on a source signal received on path 134 according to various

aspects of the present invention to generate an output voltage level which is (substantially) immune from any noise also received on path 134. Sampling circuit 210 may further perform operations such as correlated double sampling (CDS) to generate a voltage level corresponding to a pixel of image 110.

[0028] PGA 220 amplifies the voltage level received on path 212 by a gain specified typically by a designer depending on image 110. ADC 230 digitizes the amplified voltage signal to generate pixel digital elements on path 146 for further processing. PGA 220 and ADC 230 may be implemented in a known way.

[0029] The digital elements generated by ADC 230 may accurately reflect image 110 as sampling circuit 210 may be implemented to be immune to any noise present in the input signal received on path 134. Various aspects of the present invention will be clearer by first appreciating a prior approach, which may not include one or several features of the present invention. Accordingly, a prior approach is described below first.

[0030] *4. Prior Sampling Circuit*

[0031] Figure 3 is a circuit diagram illustrating the details of a sampling circuit in one prior embodiment. Sampling cir-

cuit 300 is shown containing resistor 310, capacitor 320, and switches 330, 340 and 350. Each component is described below.

[0032] Resistor 310 receives input signal (includes both source signal and a noise signal) on path 311 and provides bandwidth limiting to the input signal, as described in further detail below. Capacitor 320 samples the input signal by charging to the voltage level of input signal when switches 330 and 340 are closed. The time (Ts) duration of sampling is controlled by controlling switches 330 and 340. The voltage across capacitor 320 at the end of sampling time, Ts, represents the sampled voltage level and is provided on path 399. Capacitor 320 discharges through switch 350 when in closed state for next sampling of input signal 311.

[0033] As is well known in relevant arts, resistor 310 and capacitor 320 together operate as a low pass filter, which limits the bandwidth of input signal 311. Due to the bandwidth limiting, any high frequency CCD noise signal components are removed from signal 311 and low frequency source signal components are provided on path 399. Bandwidth limiting may be achieved by choosing R_C (Rs and C320, wherein Rs is series resistance including resistance of re-

sistor 310, and switches 330 and 340) time constant (Trc) of a desired value (as is well known in the relevant arts) to effectively reduce CCD noise signal components.

[0034] Thus, sampling circuit 300 samples source signal level received on path 311 at a time instant and provides the sampled voltage on path 399. In addition, sampling circuit 300 performs bandwidth limiting to reduce CCD noise signal components in the sampled output on path 399.

[0035] One potential problem with sampling circuit 300 is the signal at output may be degraded. The degradation may be caused as the voltage on path 399 may equal a fraction (much less than 1) of the voltage level of signal 311. The reason for such a fraction may be appreciated by understanding that the R_C time constant Trc equals the product of Rs and C320, and generally has a limited value. Due to the requirement that Trc to be greater than or equal to Ts/2, the value of Ts may also be small and capacitor 320 may charge to only a fraction of the voltage level 311 in time duration Ts. Thus, the image quality is diminished due to such partial charging.

[0036] The degradation of image quality in such a situation may be degraded by the non_linearity introduced by switch 330. At least in case of implementations using technolo-

gies such as CMOS transistors, the resistance of switch 330 varies with variation in voltage level of input signal 311. The variable resistance introduces non_linearity into the operation of sampling circuit 300 due to the partial charging. As a result, the image quality is diminished since the sampled output voltage level on path 399 is determined by R_C time constant Trc, which depends on variable resistance R310, thereby degrading the image quality. Various aspects of the present invention overcome some of such problems as described below in further detail.

[0037] *5. Sampling circuit*

[0038] Figure 4 is a circuit diagram illustrating the details of a sampling circuit in an embodiment of the present invention. Merely for illustration, sampling circuit 400 is described with reference to Figures 1 and 2, however, sampling circuit 400 can be implemented in other environments as well. Sampling circuit 400 is contained in sampling circuit 210 of Figure 2. Sampling circuit 400 is shown containing resistor 410, capacitors 420 and 440, buffer 430, and switches 450, 460, 470 and 480. Each component is described below.

[0039] Broadly, a first circuit portion containing resistor 410, ca-

pacitor 420, and switches 450/460 performs bandwidth limiting and the second circuit portion containing capacitor 440, and switches 470/480 performs sampling. As may be apparent, the first circuit portion and second circuit portions are implemented using a separate set of components. Due to the use of two separate portions for bandwidth limiting and sampling respectively, sampling circuit 400 may be substantially immune to noise in the input signal received on path 134, while providing a linear response as described below.

[0040] Switches 450, 460, 470 and 480 are controlled by a clock signal (not shown). During one phase of the clock signal, switches 460, 470 and 480 are closed and switch 450 is opened to sample input signal on path 134. During another phase of the clock signal, switches 460, 470 and 480 are opened and switch 450 is closed to enable capacitor 420 to sample next signal on path 134. The manner in which bandwidth limiting may be performed is described below first, and then sampling is described later.

[0041] Resistor 410 receives input signal on path 134 and capacitor 420 charges to the voltage level of input signal 134 when switch 460 is in closed state. Capacitor 420 discharges through switch 450 when in closed state to sam-

ple the next signal level. Upper plate of capacitor 420 is connected to resistor 410 and lower plate of capacitor 420 is connected to a common mode voltage via switch 460.

[0042] Thus, the configuration of resistor 410 and capacitor 420 operates as a low pass filter, which limits the bandwidth by removing high frequency noise signal components and allowing only low frequency source signal components to be present across capacitor 420. The noise signal may be reduced effectively by selecting RC (R410 and C420) time constant to be large. The manner in which sampling may be performed is described below.

[0043] Capacitor 440, and switches 470 and 480 together sample the voltage level of source signal (which does not include noise signal) received on path 134. Capacitor 440 samples the voltage level stored on capacitor 420 when switches 470 and 480 are closed (switch 460 is also closed on the same time) and provides the sampled voltage level on path 212 when switches 470 and 480 are opened. However, switch 470 is opened before switch 460 is opened to avoid charge injection on capacitor 440.

[0044] Buffer 430 provides a low impedance drive to the second circuit portion, and thus allowing the required drive cur-

rent to capacitor 440 to settle (substantially) completely (that is, charges to the sampled voltage level on capacitor 420). As a result, linearity of the sampled voltage level provided on path 212 may not be affected. If buffer 430 is not present, capacitor 440 loads capacitor 420 and thus causes the voltage across capacitor 420 to be reduced.

[0045] In comparison to the prior circuit described above with reference to Figure 3, it may be noted that a non_linear switch, whose resistance value changes with input signal swing, is not present in input signal path. Even though switch 470 receives input signal 134 through buffer 430, the path in which switch 470 is present operates with a small time constant (due to absence of series resistance). Thus, the non_linearity of resistance of switch 470 may not affect the sampled output on path 212. As a result, non_linearity in the sampled output signal on path 212 may be negligibly small.

[0046] However, buffer 430 needs to be capable of receiving high bandwidth of the signal present at the output of capacitor 420. Buffer 430 may also need to have bandwidth greater than RC (R410 x C420) time constant in order not to introduce error due to settling and phase shift as is well known in relevant arts. In addition, buffer 430 may need

to be capable of receiving a voltage swing as large as the voltage swing in input signal 134 since voltage stored on capacitor 420 approximately equals input voltage 134 (Vi) as given by equation (1).

[0047] Voltage on capacitor 420 = Vi (1_exp(_Ts/RC)) Equation (1)In an example embodiment, when RC time constant equals Ts/2 to reduce CCD noise, voltage on capacitor 420 equals 0.86 of input voltage 134 as given by equation (2) below.

[0048] Voltage on capacitor 420 = Vi (1_exp(_2)) = 0.86 Vi Equation (2)However, a fast buffer with high input signal swing leads to high power dissipation and is not desirable. In general, a source_follower buffer is very fast (high bandwidth) and consumes less power. However, the input swing capacity is less. Alternatively, a closed loop class_A buffer provides high bandwidth. However, such buffer introduces more noise and also requires more power. Therefore, an alternative embodiment may overcome some of such disadvantages as described below with reference to Figure 5.

[0049] *6. Alternative Embodiment*

[0050] Figure 5 is a circuit diagram illustrating the details of a sampling circuit in an alternative embodiment of the

present invention. Merely for illustration, sampling circuit 500 is described with reference to Figures 1 and 2, however, sampling circuit 500 can be implemented in other environments as well. Sampling circuit 500 is contained in sampling circuit 210 of Figure 2. Sampling circuit 500 is shown containing resistor 510, capacitors 520, 540 and 550, buffer 530, and switches 570_1 through 570_6. Each component is described below.

[0051] Broadly, a first circuit path containing capacitor 540, and switches 570_3/570_5 samples the entire input signal (including both source signal and noise signal) received on path 134, and a second circuit path containing resistor 510, capacitors 520 and 550, buffer 530, and switches 570_1, 570_2, 570_4 and 570_6 samples only the high frequency components in input signal 134. The sampled output signal is generated as a difference of the signals sampled by the two paths 591 and 592. Due to the difference, the high frequency noise signal components received on path 134 may be eliminated and sampling circuit 500 may be substantially immune to noise in the input signal received on path 134, while providing a linear response as described below.

[0052] Switches 570_1 through 570_6 are controlled by a clock

signal (not shown). During one phase of the clock signal, switches 570_2 through 570_6 are closed and switch 570_1 is opened to sample input signal on path 134. During another phase of the clock signal, switches 570_2 through 570_6 are opened and switch 570_1 is closed to enable capacitor 520 to sample next signal on path 134. The manner in which bandwidth limiting and sampling may be performed is described below.

[0053] Resistor 510, capacitor 520, and switches 570_2 and 570_1 together operate as a high pass filter as would be apparent to one skilled in the relevant art. The high pass filter filters the low frequency components in the input signal received on path 134 and provides the remaining high frequency components on path 533.

[0054] Buffer 530, capacitor 550, and switches 570_4 and 570_6 operate similar to buffer 430, capacitor 440, and switches 470 and 480 of Figure 4 respectively. Thus, capacitor 550 samples the output of the high pass filter on path 533 when switches 570_4 and 570_6 are closed and provides the sampled output on path 592 when switches 570_4 and 570_6 are opened.

[0055] Capacitor 540 samples all frequencies of input signal received on path 134, including both the source signal and

the high frequency noise components, when switches 570_3 and 570_5 are closed and provides the sampled output on path 591 when switches 570_3 and 570_5 are opened. The sampled output on path 591 contains all the frequency components in signal 134 and the output on path 592 contains only high frequency components. Therefore, the difference of outputs on paths 591 and 592 contains the sampled output with only low frequency source signal components and thus removes high frequency CCD noise components as desirable. Paths 591 and 592 are contained in path 212 of Figure 2.

[0056] As described above with equation (2) in the above illustrative example, voltage across capacitor 520 equals 0.86Vi when RC (R510 and C520) time constant is Ts/2. As a result, the remaining voltage 0.14Vi is present across resistor 510, which is the input voltage to buffer 530 on path 533. Therefore, buffer 530 may need to be capable of receiving only 14% of the swing in input voltage (Vi). As a result of the small voltage swing at the input of buffer, the power dissipation is low. Due to the small input voltage swing, a source follower buffer may be used as buffer 530. In general, a source follower has high bandwidth and thus speed of operation is also high. The manner in which

the approaches of Figure 5 can be used to implement correlated double sampling, is described below.

[0057] *7. Correlated Double Sampler*

[0058] Figure 6 is a circuit diagram illustrating the details of a correlated double sampler (CDS) used as sampling circuit 210 in CCD environments in one embodiment. CDS 600 isshown containing resistors 615 and 625, capacitors 610, 620, 640, 645, 660 and 665, and switches 670-1 through 670-9, 680-1 and 680-2.

[0059] In an embodiment, input signal received on path 134 contains reference level and relative video level, which are multiplexed in time domain. Thus, the reference level and the relative video level form the source signal in the corresponding time domain, and the input signal on path 134 contains noise signal in addition to the source signal. The actual video level may be obtained by subtracting relative video level from the reference level, as is well known in the relevant arts. The manner in which CDS 600 generates a sample representing the actual video level is described below.

[0060] Broadly, CDS 600 samples reference level during one phase (phase I) of clock signal and relative video level during another phase (phase II) of clock signal, and pro-

vides the actual video level between output paths 691 and 692. Paths 691 and 692 are contained in path 212 of Figure 2. CDS 600 may implement the approaches described above with respect to sampling circuit 500 to sample both reference level and relative video level as described below in detail.

[0061] Such a sampling operation is supported by appropriately closing and opening various switches during different phases. Thus, all the shown switches in CDS 600 may be controlled by a clock signal (not shown). Switches 680_1 and 680_2 are closed to discharge capacitors 610 and 620 respectively prior to sampling input signal 134 and generating an actual video level. The manner in which actual video level may be generated from input signal 134 while substantially eliminating noise signal is described in further detail below.

[0062] During phase I, a first circuit path containing capacitor 640, and switches 670_3 and 670_6 passes input signal received on path 134 onto capacitor 640 , the other end of which is held at a constant voltage by switch 670_6. The passed signal represents all frequency components of (reference level + high frequency noise).

[0063] A second circuit path containing resistor 625, capacitors

620 and 645, buffer 630, and switches 670_2, 670_4, and 670_7 passes input signal received on path 134 onto capacitor 645 after filtering it through the high_pass filter formed by resistor 625 and capacitor 620. The other end of capacitor 645 is held at a constant voltage by closing switch 670_7, while the second circuit path passes the input signal.

[0064] At the end of phase I , switches 670_6 and 670_7are opened. As a result, the difference in voltages across capacitors 640 and 645, which is of (all frequency components _ high frequency components) represents the low frequency component of input signal 134. Thus, the low frequency reference level (with the high_frequency noise removed) sampled across capacitors 640 and 645 differentially may be obtained.

[0065] During phase II , input signal 134 contains a reference video level, and the first circuit path passes input signal 134 onto capacitor 640. The passed signal represents all frequency components of (reference video level + high frequency noise). A third circuit path containing resistor 615, capacitors 610 and 645, buffer 635, and switches 670_1, 670_5, and 670_7 passes input signal received on path 134 after filtering it through the high_pass filter

formed by resistor 615 and capacitor 610, onto capacitor 645.

[0066] It may be noted that switches 670_6 and 670_7 are opened during phase II, thus the other end of capacitors 640 and 645is not held at a constant voltage, rather connected to the virtual ground of amplifier 650, which is in amplification mode. As a result, capacitors 640 and 645 still hold the sampled reference level during phase I across them. In addition, as capacitors 640 and 645 would be present in series with the filtered relative video level during phase II, the voltage at the output of amplifier 650 represents (low_frequency filtered relative video level sampled in phase II -low_frequency filtered reference level stored on capacitors 640 and 645in phase I), which in turn represents low_frequency actual video level with noise components removed.

[0067] Amplifier 650 amplifies the difference on paths 651 and 652 at the end of phase II due to the feedback paths formed by capacitors 660 and 665. The feed back paths are formed by capacitors 660 and 665 since switches 670_8 and 670_9 are closed during phase II. Due to charge sharing between capacitors 640 and 660 and also between capacitors 645 and 665, the difference is ampli-

fied and available for further processing on paths 691 and 692.

[0068] Thus, the difference signal between paths 691 and 692 represents the actual video level containing only low frequency components. Due to the bandwidth limiting, the output may be substantially independent of noise. In addition, linearity of response is maintained/enhanced by using various other features of the present invention.

[0069] *8. Conclusion*

[0070] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.